Quantized rectification in a quantum dot nanojunction

C. R. Müller,[1,*] L. Worschech,[1] S. Lang,[1] M. Stopa,[2] and A. Forchel[1]

[1]*Technische Physik, Physikalisches Institut, Universität Würzburg and Wilhelm Conrad Röntgen Research Center for Complex Material Systems, Am Hubland, D-97074 Würzburg, Germany*

[2]*Center for Nanoscale Systems, Harvard University, 17 Oxford Street, Cambridge, Massachusetts 02138, USA*

(Received 11 March 2009; revised manuscript received 25 June 2009; published 25 August 2009)

Rectification properties of a quantum wire (QW) coupled asymmetrically to a quantum dot (QD) are studied for bias voltages up to 1 V. The QW-QD system is based on a modulation-doped GaAs/AlGaAs heterostructure with InGaAs self-assembled quantum dots in close vicinity to a two-dimensional electron gas. Due to an applied lateral electric field, the coupled QW-QD system is formed. By increasing the bias voltage, the QD becomes charged by electron tunneling from the wire and quantized rectification is observed in the QW. We attribute the rectifying behavior to a recently proposed charging rectifier [M. Stopa, Phys. Rev. Lett. **88**, 146802 (2002)], whereas many electrons contribute to the charging rectification.

DOI: 10.1103/PhysRevB.80.075317 PACS number(s): 85.35.Be, 73.40.−c

I. INTRODUCTION

Current rectification plays an important role in electron transport and is fundamental for the development of novel basic elements in electronic circuitry. In nanostructured electronic devices with geometrical dimensions in the order of the electron mean free path, electron transport is mainly determined by reflections from the device boundaries and not by electron scattering at inherent impurities.[1] Therefore, electrons can propagate ballistically and efficient ballistic rectifiers have been proposed and demonstrated with a strong influence of the shape of the active region on the device functionality.[2–7]

In contrast to these ballistic rectifiers, which can be operated even for symmetrically designed devices, the classical approach for realizing rectifiers is due to an asymmetrical design. Hence, the working principle is based on, e.g., different doping in a *p-n* junction or the semiconductor-metal junction in a Schottky diode. Therefore, for small geometric dimensions, fabrication techniques with a high spatial resolution are required to ensure device functionality. Alternatively, rectification can be achieved by breaking the inversion symmetry of the device; systems, which are often referred to as ratchets.[8–11] However, the ultimate limit of a downscaled rectifier would be a device in which the asymmetry is realized by integrating only a single component, such as a quantum dot (QD), asymmetrically.

Here, we propose and demonstrate pronounced rectification up to several 100 mV in a nanoscaled junction due to a single QD, i.e., trap dot (TD), coupled asymmetrically to a quantum wire (QW). The rectifier, which is operated as a multiple electron charging rectifier, provides stable rectification characteristics. Multiple charging of the TD, leading to quantization in the device characteristics, is demonstrated even in the strong nonlinear transport regime, i.e., for bias voltages up to 1 V. Our system is based on a modulation-doped GaAs/AlGaAs heterostructure with InGaAs self-assembled quantum dots (SAQDs) which are situated in close vicinity to a two-dimensional electron gas (2DEG). In particular, a Y-branch switch (YBS) (Refs. 12–16) was driven as a two-terminal conductor. This was achieved by charging the SAQDs, which results in a local depletion of one branch and isolates this branch electrically from the QW. The branch serves as TD and controls the transport properties of the QW by Coulomb interactions between the electrons in the TD and the electrons in the QW. Such charging rectifiers have been proposed and demonstrated for the quadruple point,[17,18] i.e., only one electron can access the system at a time. Charging rectifiers beyond the quadruple point would allow to realize devices with large output signals, which may serve as sensors for external electric and magnetic field, charge-read-out detectors operating in the strong nonlinear transport regime or even for spin-based electronic devices.

II. DEVICE FABRICATION

The charging rectifier is based on a modulation-doped GaAs/AlGaAs heterostructure with InGaAs SAQDs in the spacer. A schematic cross section of the layer sequence grown by molecular-beam epitaxy is shown in Fig. 1(a). Based on a semi-insulating GaAs substrate, a 200-nm-thick GaAs buffer followed by a tenfold superlattice, consisting of an alternating sequence of 25-nm-thick $Al_{0.2}Ga_{0.8}As$ and 10-nm-thick GaAs layers, was deposited. On top of this, 2 μm

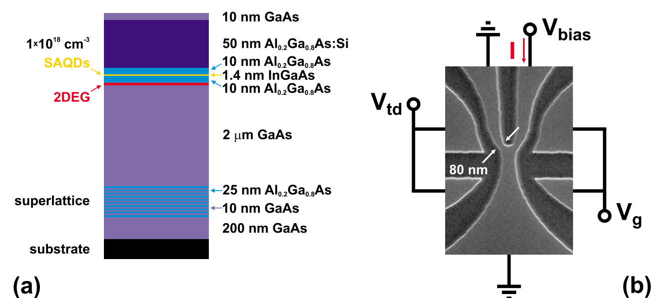

FIG. 1. (Color online) (a) Schematic cross section of the GaAs/AlGaAs heterostructure with InGaAs SAQDs. The SAQDs are located approximately 10 nm away from the 2DEG in the center of the $Al_{0.2}Ga_{0.8}As$ spacer. (b) SEM image of the studied sample together with the electric setup.

 ©2009 The American Physical Society

GaAs and a 20-nm-thick $Al_{0.2}Ga_{0.8}As$ spacer were grown and the heterostructure was completed by a 50-nm-thick Si-doped $Al_{0.2}Ga_{0.8}As$ layer. The Si concentration was 1×10^{18} cm^{-3} and the Si-doped $Al_{0.2}Ga_{0.8}As$ layer is capped by a 10-nm-thick GaAs layer.

At the heterostructure interface, a 2DEG is formed, which resides approximately 80 nm below the sample surface. By depositing 1.4 nm InGaAs, SAQDs with a density of 5×10^{10} cm^{-2} and a diameter of 25 nm were formed due to Stranski-Krastanov growth mode in the center of the spacer. The SAQDs were situated in close vicinity to the 2DEG and are only separated by the lower, 10-nm-thick part of the $Al_{0.2}Ga_{0.8}As$ spacer from the 2DEG. Hall measurements performed at $T=4.2$ K provided an electron density of $n_{2DEG} = 4 \times 10^{11}$ cm^{-2} and an electron mobility of $\mu_e = 8.5 \times 10^3$ cm^2/Vs in the 2DEG. The SAQDs deplete the nearby 2DEG and antidots are formed in the 2DEG. These antidots act as additional scattering centers and, thus, the electron mobility is reduced strongly.[19]

A YBS with four isolated side gates was defined by 110-nm-deep and 250-nm-wide etched trenches by using electron-beam lithography and wet-etching techniques. Figure 1(b) shows a scanning-electron microscope (SEM) image of the sample together with a sketch of the electric setup. Close to the branching point, the minimum constriction of the branches is about 80 nm. Stem and left branch were both connected to ground, whereas a bias voltage V_{bias} was applied to the right branch. The gate voltages V_{td} and V_g were applied to the side gates close to the left and right branch, respectively.

Due to Coulomb repulsion between the charged SAQDs and the electrons in the 2DEG, the 2DEG is locally depleted beneath the SAQDs in the order of the screening length ($\sim$50 nm). Transport measurements performed with comparable structures indicate that coupled electron islands are formed in the 2DEG.[20,21] Figure 2(a) shows such a scenario schematically with a QW situated between the stem reservoir and the reservoir of the right branch. In the left branch, an electron island is formed close to the branching point in the constrained 2DEG. This electron island, or TD, is separated from the QW by a potential barrier.

III. POSITIONING OF THE TRAP DOT

To verify the formation of an isolated TD in the 2DEG, both experimental and numerical methods were used. By performing transport measurements in the linear transport regime, the differential conductance of the YBS was determined. The YBS was operated as two-terminal device and, due to different electric setups, a transport channel was located between stem and left branch (mode 1), stem and right branch (mode 2), and left branch and right branch (mode 3). For bias voltages up to ± 20 mV, Coulomb blockade has been observed in modes 1 and 3 whereas in mode 2 no Coulomb blockade oscillations have been found (not shown). Therefore, we conclude that an electron island, serving as TD, is formed only in the left branch.

In addition to this experimental approach, Fig. 2(b) displays the modeled, effective potential of the 2DEG in a YBS with two QDs positioned in the spacer above one of the branches. For the calculation, the position of the QDs was arbitrarily chosen and the occurrence of intrinsic disorder was neglected. The results are based on an electronic structure similar to the grown modulation-doped GaAs/AlGaAs heterostructure used for the device. The calculation is based on the solution of the Schrödinger equation in the z direction, i.e., along the axis of growth. For each point in the x-y plane, the Thomas-Fermi approximation was used and, thus, the calculation is quasi-adiabatic. Charged QDs were assumed in the spacer between the donor layer and the 2DEG and a lateral confinement has been implemented by metal gates on the surface of the system. As one can clearly see, in the center of the YBS, the effective potential is low and increases toward the boundaries of the device. Directly underneath the two QDs, the effective potential is raised and two antidots are formed. The electrons which are situated in between these antidots are, on the one hand, electrically (i.e., Ohmically) isolated from the QW and, on the other hand, from the corresponding branch reservoir as well.

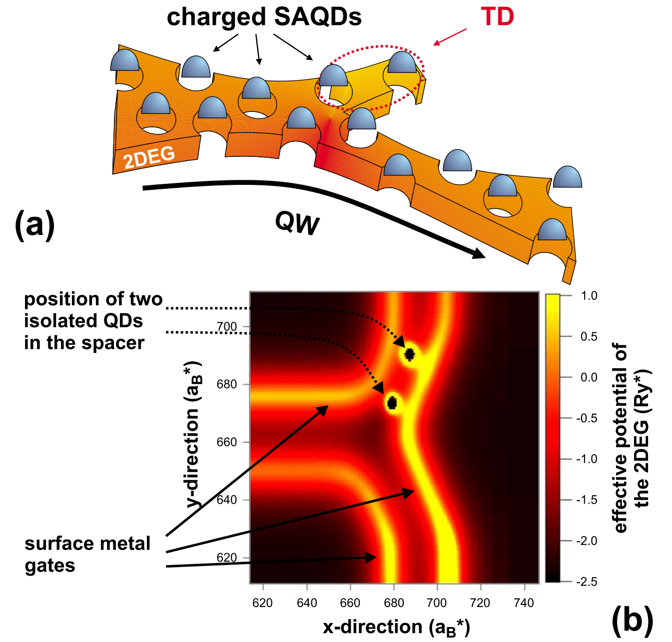

FIG. 2. (Color online) (a) Below charged SAQDs, the conduction band is raised, which results in depleted areas (indicated schematically by holes in the 2DEG) and, due to lateral confinement, a TD is formed in the left branch. (b) Calculation of the effective potential of the 2DEG in a YBS with two QDs placed in the spacer above one of the branches in units of the effective Rydberg constant R_y^* ($1R_y^* \simeq 5.83$ meV). The system dimensions are given in units of the effective Bohr radius a_B^* ($1a_B^* \simeq 9.8$ nm).

Hence, a TD, isolated by potential barriers, is formed by charged SAQDs and the lateral confinement of the branch. Based on the dot density, one can conclude that a maximum number of five to seven SAQDs are situated in the left branch and close to the branching point. The average dot distance in the spacer is approximately 50 nm and, therefore, smaller than the one used for the calculation. With respect to the self-assembled nature of the QDs in our system, also a bunch of close-by SAQDs should be regarded as possible

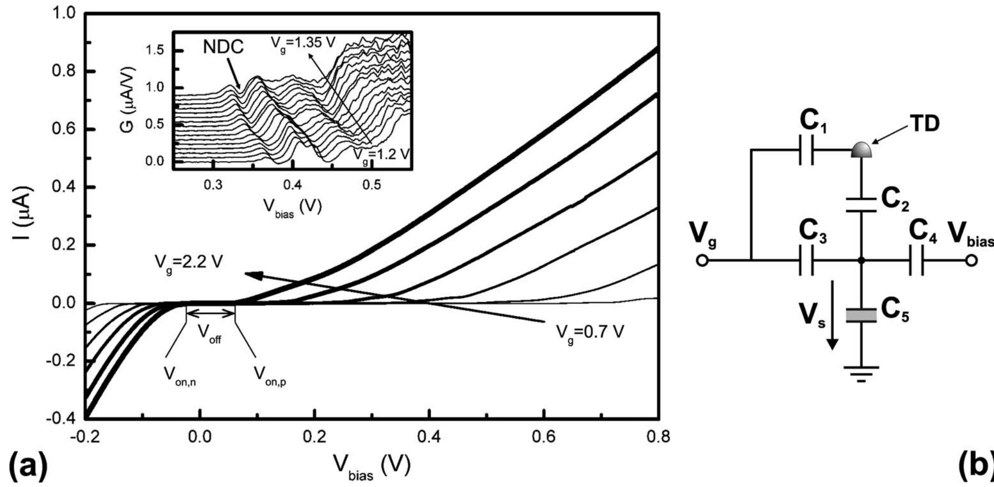

FIG. 3. (a) Current I versus the applied bias voltage V_{bias} for different gate voltages V_g. The cutoff voltage V_{off} characterizes the bias range in which no electron transport occurs. The onset voltages $V_{on,p}$ and $V_{on,n}$ define the bias points at which the current flow sets in for positive and negative bias, respectively. Inset: Differential conductance G versus V_{bias} for V_g from 1.2 to 1.35 V. (b) Capacitive equivalent network of the QW-QD system.

origin of the isolating potential barriers. However, the numerical calculations support our experimental findings and lead to the conclusion that a TD can form in one branch due to a charging of the SAQDs.

IV. DEVICE CHARACTERISTICS

For the measurements, $V_{td}=-1.0$ V was tuned in a way that for $0.5<V_g<2.25$ V no current flows through the left branch with $-1.0<V_{bias}<1.0$ V. Such a system resembles the charging rectifier proposed by Stopa for a QW coupled asymmetrically to a TD.[17] Here, in the experimental setup, V_{bias} was increased from −0.2 to 0.8 V and the current I was measured. V_{bias} was swept for constant V_g and the measurements were repeated several times with V_g increased in steps of 10 mV from 0.5 to 2.25 V.

All measurements were performed in the dark at 4.2 K with the sample immersed in liquid helium and started about 15 min after inserting the sample into the liquid helium. Prior to the transport measurements, a voltage pulse of $V_g=V_{td}=-3.5$ V was applied for 5 s to all side gates with $V_{bias}=0$. This leads to a controlled charging of the SAQDs[22,23] and provides comparable charge states for every cooling down of the sample. To verify our findings, several YBSs with different designs were studied. The results reported here were observed for different samples and also for different cooling down cycles. Large fluctuations in the device characteristics as reported, e.g., for bias cooled devices were not found.[24]

The current I versus V_{bias} is shown in Fig. 3(a) for V_g =0.7, 1.0, 1.3, 1.6, 1.9, and 2.2 V. For $V_g=2.2$ V, I is negative at small V_{bias} and increases monotonically with increasing V_{bias}. For $V_{bias}>-0.015$ V, the channel is cut off and no current flows until V_{bias} reaches a value of 0.05 V. Bias voltages larger than 0.05 V lead to a rising of I with a maximum value of $I=0.9$ μA for $V_{bias}=0.8$ V. The cutoff voltage V_{off} characterizes the bias voltage range in which no current flows [as indicated in Fig. 3(a)] and is defined by the difference of the onset voltages $V_{on,p}$ and $V_{on,n}$ of the QW for positive and negative bias, respectively.

The inset of Fig. 3(a) shows the differential conductance G versus V_{bias} for V_g from 1.2 to 1.35 V in steps of 10 mV. For clarity, the curves were offset with increasing V_g. For $V_g=1.2$ V, the differential conductance is zero for bias voltages smaller than 0.35 V. With increasing bias voltage, G is enhanced and peaks are observed for $V_{bias}=0.37$, 0.41, 0.43, and 0.47 V. In between these peaks, negative differential conductance (NDC) occurs at $V_{bias}=0.38$ and 0.44 V. With increasing V_g, the position of both peaks and NDC is shifted toward smaller bias voltages.

The left-hand side of Fig. 4 displays the onset voltages $V_{on,p}$ and $V_{on,n}$ versus V_g. For positive bias, $V_{on,p}$ decreases from 0.75 to 0.05 V with increasing gate voltage. Interestingly, in the decrease of $V_{on,p}$, steps appear for $V_g=0.68$, 1.06, 1.46, and 1.84 V. In between these steps, $V_{on,p}$ decreases linearly with a larger slope for smaller gate voltages.

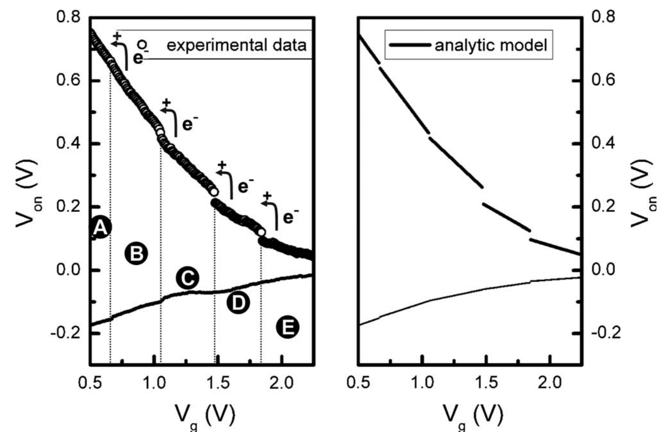

FIG. 4. Experimentally determined onset voltages $V_{on,p}$ and $V_{on,n}$ together with the analytic modeling versus V_g. Regions A to E mark the gate voltage ranges used to distinguish different charge states of the TD.

TABLE I. Capacitances C_2 and C_4 determined according to Eqs. (2) and (3) for different ranges of the gate voltage V_g.

	A	B	C	D	E
C_2(F)	2.5×10^{-20}	2.7×10^{-20}	4.1×10^{-20}	9.3×10^{-20}	1.3×10^{-18}
C_4(F)	9.2×10^{-19}	9.7×10^{-19}	1.4×10^{-18}	2.4×10^{-18}	5.1×10^{-18}

The spacing between the steps is almost equidistant. For negative bias, $V_{on,n}$ increases from −0.18 to −0.02 V with increasing V_g. Also here, steps can be observed at the above mentioned gate voltages. In contrast to $V_{on,p}$, the slope of the $V_{on,n}$-V_g curve is reduced by a factor of 4, compared to the value for $V_{on,p}$, in between these steps.

We relate the observed rectification, i.e., the nonlinearity in the I-V_{bias} characteristics, which comes along with large differences in the onset voltages $V_{on,p}$ and $V_{on,n}$, to a change in the charge state of the TD. For negative bias, electron injection into the TD is suppressed and the charge state of the TD is not altered. For positive bias, the electron flow is inverted and electrons can propagate from the stem region either into the right branch or the TD. For a charging of the TD, the potential barrier in the constriction of the QW is increased due to the Coulomb interaction. This increase leads to an abrupt reduction in the conductivity of the QW and the onset voltage is shifted. Due to the fact that the TD is not totally discharged, a nonzero onset voltage is observed even for negative bias. With increasing gate voltage, the probability for electrons to propagate from the stem region into the TD is reduced due to the increasing lateral electric field and the charge state of the TD is lowered. Hence, the onset voltages of both negative and positive bias show distinct steps with increasing gate voltage and the rectification is quantized. The increase in the potential barrier in the QW is in proportion to the number of electrons in the TD. Hence, the more electrons the TD can carry, the more pronounced the rectification is, i.e., the differences in the onset voltages. Evidently, due to the stability of the system, the rectifier can be operated far beyond the quadruple point. Thus, both multiple charging of the TD as well as many electrons contributing to the current flow are allowed. In addition to the shift of the onset voltages, an additional electron in the TD leads to an abrupt reduction in the conductivity and NDC occurs. For a fixed gate voltage, the occurrence of several NDCs indicates a multiple charging of the TD.

V. CAPACITOR MODEL

We have modeled the capacitive coupling of the charging rectifier by an equivalent network shown in Fig. 3(b). The gate voltage controls both the TD via the capacitance C_1 as well as the constriction in the QW, i.e., the potential barrier, via the capacitance C_3. The capacitances C_2 and C_4 describe the capacitive couplings of the TD and the port at which V_{bias} is applied, respectively, with the potential barrier. The switching voltage V_s is the voltage drop across the quantum capacitance C_5 in the QW. This voltage drop corresponds to the difference between the electrostatic potential and the electrochemical potential in the QW and determines, e.g., the cutoff condition or the ideality factor of the device.[25–27] Solving this capacitive network leads to

$$\left[C_2^2-(C_1+C_2)\sum_{i=2}^{5}C_i\right]V_s=-neC_2+(C_1+C_2)C_4V_{bias}+\frac{1}{2}\left[\sum_{j=1}^{3}\sum_{k=1}^{3}\left(C_jC_k-\frac{1}{3}C_j^2\right)\right]V_g, \tag{1}$$

with e the electron charge and n the number of electrons in the TD. For $V_s=0$, no electrons are in the QW and, thus, the device is operated in the cutoff region. Therefore, for positive bias, the onset voltage of the QW is

$$V_{on,p}=-\frac{\frac{1}{2}\left[\sum_{j=1}^{3}\sum_{k=1}^{3}\left(C_jC_k-\frac{1}{3}C_j^2\right)\right]V_g-neC_2}{(C_1+C_2)C_4}. \tag{2}$$

According to Eq. (2), $V_{on,p}$ depends linearly on V_g and shifts toward smaller values of V_{bias} with increasing V_g. For a given V_g, a certain amount of electrons in the TD can inhibit electron transport through the QW. Thus, with increasing n, the onset voltage shifts to more positive voltages. For a single electron added to the TD, this charge induced shift of $V_{on,p}$ is given by

$$\Delta V_{on,p}=\frac{eC_2}{(C_1+C_2)C_4}. \tag{3}$$

The capacitance C_3 was determined from QWs fabricated with a similar epitaxial growth. In such systems, the gate capacitance is about 0.5 aF.[20] Transport measurements on YBSs showed that the capacitive coupling between side gates and the opposing branch is reduced to about 25% of C_3, i.e., $C_1=C_3/4$.

Table I shows the calculated values of C_2 and C_4 for the different ranges of V_g. Both capacitances increase with increasing gate voltage and reach maximum values in the order of aF. Large values of C_4 are associated with a potential barrier in the QW which is situated close to the electron reservoir of the right branch. So, with increasing V_g, the position of the potential barrier shifts from the branching point more into the right branch. The increase of C_2 corresponds to an enhanced capacitive coupling of the TD on the QW. Such a dynamic change is related to a reduction of the effective distance between the QW and the TD. With increasing V_g, the TD shifts from the left branch toward the branching point. This leads to an enhanced Coulomb repulsion of the electrons in the TD on the electrons in the QW.

In Fig. 4, the experimental data (left part) and analytic modeling (right part) of $V_{on,p}$ and $V_{on,n}$ are shown with the capacitances C_2 and C_4 extracted for the different gate voltage ranges (as indicated). For the calculation, the slope in the $V_{on,p}$-V_g curve in between two consecutive steps and an average step height of $\Delta V_{on,p}=30$ mV were determined. In between two steps, the charge state of the TD is constant and the onset voltage shifts linearly with V_g. The charge state of the TD is changed with every step and, as shown in Table I, also the capacitive couplings alter. The calculation of $V_{on,n}$ is based on Eqs. (2) and (3). In contrast to $V_{on,p}$, $V_{on,n}$ increases linearly for larger V_g and, thus, the sign of Eq. (2) is inverted for negative bias. The slope of the $V_{on,n}$-V_g curve is reduced by a factor of 4 compared to $V_{on,p}$. This reduction is related to an increase of C_4 also by a factor of 4 for negative bias. For the calculation of $V_{on,n}$, the above mentioned values were used for C_1, C_2, and C_3. Compared to $V_{on,p}$, the average step height $\Delta V_{on,n}$ is smaller than $\Delta V_{on,p}$, which follows directly from Eq. (3). We attribute this increase of C_4 for negative bias to a reduction of the effective width of the potential barrier in the QW. The capacitance of a potential barrier, which can be described as a leaky nano-capacitor, depends strongly on its width and increases for narrow barriers[28,29]

VI. SUMMARY

In summary, we have demonstrated a charging rectifier with pronounced rectification up to several 100 mV in a nanojunction. The rectifier was realized by coupling a TD asymmetrically to a QW and is operated as a multiple electron charging rectifier far beyond the quadruple point. Even in the strong nonlinear transport regime, stable rectification characteristics and multiple charging of the TD were observed. The rectification depends strongly on the charge state of the TD. Jumps in the onset voltage indicate single electron charging of the TD which leads to quantization in the device characteristics. Single electron discharging of the TD as well as gate-voltage-dependent dynamic capacitive couplings in the nanojunction were demonstrated and verified by modeling.

ACKNOWLEDGMENTS

The authors are grateful for financial support from the Bundesministerium für Bildung und Forschung of the Federal Republic of Germany through the nanoQUIT project. Expert technical assistance by M. Emmerling is gratefully acknowledged.

*Corresponding author; christian.mueller@physik.uni-wuerzburg.de

[1] S. de Haan, A. Lorke, J. P. Kotthaus, W. Wegscheider, and M. Bichler, Phys. Rev. Lett. **92**, 056806 (2004).
[2] R. Šordan and K. Nikolić, Phys. Rev. B **54**, 10332 (1996).
[3] A. M. Song, A. Lorke, A. Kriele, J. P. Kotthaus, W. Wegscheider, and M. Bichler, Phys. Rev. Lett. **80**, 3831 (1998).
[4] R. Fleischmann and T. Geisel, Phys. Rev. Lett. **89**, 016804 (2002).
[5] H. Q. Xu, Appl. Phys. Lett. **78**, 2064 (2001).
[6] J. Mateos, B. G. Vasallo, D. Pardo, T. González, E. Pichonat, J.-S. Galloo, S. Bollaert, Y. Roelens, and A. Cappy, IEEE Electron Device Lett. **25**, 235 (2004).
[7] M. Knop, U. Wieser, U. Kunze, D. Reuter, and A. D. Wieck, Appl. Phys. Lett. **88**, 082110 (2006).
[8] P. Reimann, M. Grifoni, and P. Hänggi, Phys. Rev. Lett. **79**, 10 (1997).
[9] H. Linke, T. E. Humphrey, A. Löfgren, A. O. Sushkov, R. Newbury, R. P. Taylor, and P. Omling, Science **286**, 2314 (1999).
[10] J. Lehmann, S. Kohler, P. Hänggi, and A. Nitzan, Phys. Rev. Lett. **88**, 228305 (2002).
[11] V. S. Khrapai, S. Ludwig, J. P. Kotthaus, H. P. Tranitz, and W. Wegscheider, Phys. Rev. Lett. **97**, 176803 (2006).
[12] T. Palm and L. Thylén, Appl. Phys. Lett. **60**, 237 (1992).
[13] Jan-Olof J. Wesström, Phys. Rev. Lett. **82**, 2564 (1999).
[14] A. N. Andriotis, M. Menon, D. Srivastava, and L. Chernozatonskii, Appl. Phys. Lett. **79**, 266 (2001).
[15] S. Reitzenstein, L. Worschech, P. Hartmann, M. Kamp, and A. Forchel, Phys. Rev. Lett. **89**, 226804 (2002).
[16] G. M. Jones, C. H. Yang, M. J. Yang, and Y. B. Lyanda-Geller, Appl. Phys. Lett. **86**, 073117 (2005).
[17] M. Stopa, Phys. Rev. Lett. **88**, 146802 (2002).
[18] A. Vidan, R. M. Westervelt, M. Stopa, M. Hanson, and A. C. Gossard, Appl. Phys. Lett. **85**, 3602 (2004).
[19] K. H. Schmidt, M. Versen, U. Kunze, D. Reuter, and A. D. Wieck, Phys. Rev. B **62**, 15879 (2000).
[20] A. Schliemann, L. Worschech, S. Reitzenstein, S. Kaiser, and A. Forchel, Appl. Phys. Lett. **81**, 2115 (2002).
[21] C. R. Müller, L. Worschech, J. Heinrich, S. Höfling, and A. Forchel, Appl. Phys. Lett. **93**, 063502 (2008).
[22] C. R. Müller, L. Worschech, A. Schliemann, and A. Forchel, IEEE Electron Device Lett. **27**, 955 (2006).
[23] C. R. Müller, L. Worschech, and A. Forchel, Phys. Rev. B **79**, 205307 (2009).
[24] S. W. Lin, J. Du, C. Balocco, Q. P. Wang, and A. M. Song, Phys. Rev. B **78**, 115314 (2008).
[25] S. Luryi, Appl. Phys. Lett. **52**, 501 (1988).
[26] D. L. John, L. C. Castro, and D. L. Pulfrey, J. Appl. Phys. **96**, 5180 (2004).
[27] J. Knoch, W. Riess, and J. Appenzeller, IEEE Electron Device Lett. **29**, 372 (2008).
[28] T. Christen and M. Büttiker, Phys. Rev. Lett. **77**, 143 (1996).
[29] X. Zhao, J. Wang, and H. Guo, Phys. Rev. B **60**, 16730 (1999).